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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,333	OKUMURA, HIROSHI	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14,16 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13, 14, 16 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/24/06 has been entered.

Response to Amendment

Amendment 6/5/06 has been entered in light of said RCE. Comments on Remarks are included below under "Response to Arguments".

Information Disclosure Statement

The examiner has considered the item listed in the Information Disclosure Statement filed May 16, 2006. A signed copy of Form PTO-1449 is herewith enclosed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 29, 16, 33 and 34*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view Yanai et al (US

2003/0025127 A1) (previously cited) and Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05 and previously cited).

Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307.

Prior Art as admitted by Applicant does not necessarily teach the further limitations

(a) "wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode";

(b) "wherein said second thin film transistor further comprises a third gate electrode formed between said second active layer and said second gate electrode";

(c) "wherein said third gate electrode has the same thickness as said first gate electrode";

(d) "wherein said third gate electrode is made of the same material as said first gate electrode".

However, *the limitation "formed in a self-aligning manner with respect to said gate electrode"* only has patentable weight in the result for the final structure and constitutes a product-by-process limitation and is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case, forming impurity doping regions in a self-aligning manner is known to strongly reduce the overlap between gate and source/drain regions. However, the claim does not quantify this reduction, neither does the specification quantify the difference between gate source/drain overlap with and without self-alignment using the gate as mask, because said overlap can be 0.1 microns when self-alignment is used and is allowed to vary between 0 and 2.0 microns if self-alignment is not used, as witnessed by claims 13 and 30. Therefore, no definite property of the final structure is implied by the step of forming the impurity doping regions (see rejection above under 35 USC 112, second paragraph). Because no definite final structure ramification can be discerned no patentable weight is given to the limitation "formed in a self aligning manner".

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

Also, it would have been obvious to include the further limitation ad (c) in view of Nakamura as well, because electrode 13 as taught by Nakamura is as a gate reduce gate – source/drain overlap, as witnessed by section [0070] (see computerized translation), so as to reduce parasitic capacitance in order to increase speed capability

([0009]) and hence is similar in its requirements to the first transistor with source/drain regions formed in a self-aligned manner. Because of the similar functional requirements the same physical dimensions may be applied. The requirement of equal thickness of the first and third electrode is in essence a range limitation of a thickness difference being zero. Applicant is in this regard reminded that Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. *Motivation* to include the teaching by Nakamura also in this regard stems from the considerations above but also from the efficiency gained by not changing a parameter that suits both transistors' requirements.

Finally, it would have been obvious to include the limitation as (d) in view of Yanai et al, who teach gate electrodes at different altitude from the substrate and pertaining to different voltage ranges for their operation still to be made of the same material (Figures 2A and 2B and [0015]). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

On claim 16: at least one of said impurity doping regions that overlap said second gate electrode includes an LDD structure 14 (see English abstract in Nakamura), which would have been obvious to include in the prior art as admitted by

Applicant because LDD regions counteract hot electron effects. *Motivation* to include the teaching on LDD structure by *Nakamura* is the avoidance of hot electron effects in the high-voltage transistor.

On claim 33: in the prior art as admitted by applicant said second gate insulating film comprises said first insulating film 303 and a gate cover film 306 formed above said first gate insulating film.

On claim 34: said first gate electrode 304, said second gate electrode 307 in the prior art as admitted by applicant are formed under wires which connect to said impurity doping regions 305a and 305b, respectively. Inclusion of the third gate electrode (as shown would have been obvious over Nakamura) necessarily places said gate electrode between the active layer and the second gate electrode according to claim 29 and hence places said third gate electrode also under said wires that connect to said impurity doping regions.

2. ***Claim 30*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view Izawa et al (5,053,849) and Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05 and previously cited).

Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first

active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307.

Prior Art as admitted by Applicant does not necessarily teach the further limitations

(a) "wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode";

(b) "wherein said second thin film transistor further comprises a third gate electrode formed between said second active layer and said second gate electrode";

(c) "wherein said impurity doping regions which overlap said second gate electrode are formed so as to overlap said second gate electrode by 2.0 μm or less".

However, *the limitation and (a), "formed in a self-aligning manner with respect to said gate electrode",* only has patentable weight in the result for the final structure. In reference to the claim language referring to "formed in a self-aligning manner with respect to said gate electrode" constitutes a product-by-process limitation and is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case, forming impurity doping regions in a self-aligning manner is known to strongly reduce the overlap between gate and source/drain regions. However, the claim does not quantify this reduction, neither does the specification quantify the difference between gate source/drain overlap with and without self-alignment using the gate as mask, because said overlap can be 0.1 microns when self-alignment is used and is allowed to vary between 0 and 2.0 microns if self-alignment is not used, as witnessed by claims 13 and 30. Therefore, no definite property of the final structure is implied by the step of forming the impurity doping regions (see rejection

above under 35 USC 112, second paragraph). Because no definite final structure ramification can be discerned no patentable weight is given to the limitation "formed in a self aligning manner".

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

Finally, it would have been obvious to include the further limitation ad (c) in view of Izawa et al, who, in a patent on overlapping gate/drain gate structures (see title), hence analogous art, teach the overlap to be about 0.2 mm (col. 13, l. 53-66), which overlaps the range as claimed. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

1. ***Claim 31*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view Numasawa et al (6,048,795) and Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05 and previously cited).

Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304) formed above said insulating substrate (cf. Figure 1), wherein said first thin film transistor comprises a first active layer 302 (island-like portion to the left in Figure 1; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second active layer, a second gate electrode formed 307 (see [03]) on said second gate insulating film,

wherein a thickness of said second gate insulating film 303/306 is larger than a thickness of said first gate insulating film 303, by the thickness of 306 (see [03]),

wherein said second active layer 302 has at least two impurity doping regions 305b (see [03]) which overlap said second gate electrode 307.

Prior Art as admitted by Applicant does not necessarily teach the further limitations

(a) "wherein said first active layer has at least two impurity doping regions formed in a self-aligning manner with respect to said first gate electrode";

(b) "wherein said second thin film transistor further comprises a third gate electrode formed between said second active layer and said second gate electrode";

(c) "wherein said third gate electrode comprises a two-layer structure including a semiconductor layer and a metal or a metal silicide layer".

However, *the limitation and (a), "formed in a self-aligning manner with respect to said gate electrode",* only has patentable weight in the result for the final structure. In reference to the claim language referring to "formed in a self-aligning manner with respect to said gate electrode" constitutes a product-by-process limitation and is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case, forming impurity doping regions in a self-aligning manner is known to strongly reduce the overlap between gate and source/drain regions. However, the claim does not quantify this reduction, neither does the specification quantify the difference between gate source/drain overlap with and without self-alignment using the gate as mask, because said overlap can be 0.1 microns when self-alignment is used and is allowed to vary between 0 and 2.0 microns if self-alignment is not used, as witnessed by claims 13 and 30. Therefore, no definite property of the final structure is implied by the step of forming the impurity doping regions (see rejection above under 35 USC 112, second paragraph). Because no definite final structure ramification can be discerned no patentable weight is given to the limitation "formed in a self aligning manner".

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode 13 between an active layer and a gate electrode 17 with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

Finally, it would have been obvious to include the further limitation ad (c) in view of Numasawa et al, who, in a patent on gate electrodes formed in a self-alignment process step with source and drain regions (see Figure 2E and col. 1, l. 17-52), hence analogous art, teach the gate electrode to comprise a two –layer structure including a

semiconductor layer 13 and a metal layer 14 (col. 3, l. 25 – col. 4, l. 58). *Motivation* to include the teaching by Numasawa et al in the invention of the Prior Art derives from the advantage of increased electric conductivity of the gate electrode without having to give up the convenience of the self-alignment process step in creating source and drain regions with the gate as mask (col. 1, l. 16-30).

2. ***Claim 32*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Yanai et al and Nakamura as applied to claim 29 above, and further in view of Izawa et al (5,053,849).

As detailed above, claim 29 is unpatentable over Prior Art admitted by Applicant in the specification, in view of Yanai et al and Nakamura, none however teaching the further limitation as defined by claim 32. However, it would have been obvious to include said further limitation in view of Izawa et al, who, in a patent on transistor gates with gate/drain overlap, teach the gate electrode to comprise a semiconductor layer, in particular two polysilicon layers 3 and 5 (Figures 1c, 6B, e.g; and abstract and col. 4, l. 4 – col. 5, l. 2), in order to being able to better control said gate/drain overlap. *Motivation* to include the teaching by Izawa et al in the invention as admitted by applicant in the specification derives from the better control of the amount of overlap, thus ensuring better control of the operational characteristics of the transistor.

3. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Yanai et al and Nakamura as applied to claim 29 above, and further in view of of Adler et al (5,757,050) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as admitted by Applicant, in view of Yanai and

Nakamura, none necessarily teaching the further limitation defined by claim 13. However, it would have been obvious to include said further limitation in view of Adler et al who teach a thin film transistor that is self-aligned (col. 2, l. 50-59) and with overlap by 0.1 mm or less (col. 8, l. 24-43). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

4. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Yanai et al and Nakamura as applied to claim 29 above, and further in view of Zhang et al (6,507,069 B1) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as admitted by Applicant in view of Yanai and Nakamura, none however necessarily teaching the further limitation defined by claim 14. However, it would have been obvious to include said further limitation in view of Zhang et al, who, in a patent on thin film transistors, hence analogous art, teach self-aligned thin film transistors to include LDD regions for the specific reason to reduce the OFF current (col. 2, l. 9-15). *Motivation* to include the teaching by Zhang thus derives from the obvious advantage to reduce the inherently unwanted current in the OFF state.

Response to Arguments

Continued examination has prompted reconsideration of the indication of allowable subject matter in the previous action, with apologies by examiner. The central problem is the absence, in the specification, of a separation between the ranges for the overlap between gate and impurity doping regions with and without self-alignment. As indicated previously, the limitation "formed in a self-aligning manner" in itself has no patentable weight. Figures in the application show the well-known consequence of self-alignment, i.e., the inner edges of the impurity doping regions in the active layer being flush with the gate edges. However, applicant, in the specification admits overlapping ranges for said overlap between transistors made with self-alignment and without, i.e., less than 0.1 μm and less than 2 μm, respectively. Examiner concludes that the distinction between with and without self-alignment does not necessarily have any consequences for the transistors thus built in their final structure. In a further correction examiner corrects having referred to the limitation as a functional limitation; instead it is a product-by-process limitation. The rejections provided overleaf were prompted by this consideration.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
September 19, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)